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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,704	02/13/2004	Yoshitaka Nakamura	Q79889	5693

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EXAMINER	
DICKEY, THOMAS L	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 05/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding..

Office Action Summary	Application No.	Applicant(s)	
	10/777,704	NAKAMURA ET AL.	
	Examiner	Art Unit	
	Thomas L. Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,3,8,9,15,16,18-20 and 49-62* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *3,9 and 53-62* is/are allowed.

6)☒ Claim(s) *2,8,15,16,18-20,49,50 and 52* is/are rejected.

7)☒ Claim(s) *51* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 3/29/06 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 2,8,15,16,18-20,49,50 and 52 are rejected under 35 U.S.C. 102(b) as being anticipated by TORII et al. (6,380,574).

A. With regard to claims 2,15,16, and 18-20 the third example of Torii et al. discloses a semiconductor device comprising memory cells each having an MISFET for memory selection formed on a major surface of a semiconductor substrate 21 and a capacitive

element comprised of a ruthenium metal film (note column 8 line 66 and column 9 line 15) lower electrode 164-181 electrically connected at a bottom portion 164 to one of a source and drain 25 and 26 of said MISFET for memory selection via a titanium nitride film (note column 8 line 65) first metal layer 101 and a ruthenium film upper electrode 132 formed on said lower electrode 164-181 via a tantalum oxide (although Torii et al. write of using SBT in example 3, they make clear, note column 3 lines 19-23, that tantalum oxide is interchangeable with SBT in the disclosed examples) capacitive insulating film 131, wherein said lower electrode 164-181 has a cup shape provided along a side wall portion of a hole in an interlayer insulating film 161-171 (Torii et al. make their interlayer insulating film in two steps, covering the lower film 161 of figure 16 with an upper film 171 in figure 17) and a bottom portion of the hole provided in the interlayer insulating film 161-171, and has a bottom portion 164 of said lower electrode 164-181 having a thickness (60 nm, note column 8 line 66) greater than a side wall portion 181 (only 50 nm thick, note column 9 line 50) of said lower electrode 164-181. Note figures 2,3,14-19, column 3 lines 19-23, column 8 lines 14-67, and column 9 lines 1-45 of Torii et al.

B. With regard to claims 8,15,16, and 18-20 the third example of Torii et al. discloses a semiconductor device comprising memory cells each having an MISFET for memory selection formed on a major surface of a semiconductor substrate 21 and a capacitive element comprised of a ruthenium metal film (note column 8 line 66 and column 9 line 15) lower electrode 164-181 electrically connected at a bottom portion 164 to one of a

source and drain 25 and 26 of said MISFET for memory selection via a titanium nitride film (note column 8 line 65) first metal layer 101 and a second metal layer 162; and a ruthenium film upper electrode 132 formed on said lower electrode 164-181 via a tantalum oxide (although Torii et al. write of using SBT in example 3, they make clear, note column 3 lines 19-23, that tantalum oxide is interchangeable with SBT in the disclosed examples) capacitive insulating film 131, wherein said lower electrode 164-181 has a cup shape provided along a side wall portion and a bottom portion of a hole provided in an interlayer insulating film 161-171 (Torii et al. make their interlayer insulating film in two steps, covering the lower film 161 of figure 16 with an upper film 171 in figure 17), said first metal layer 101 and said second metal layer 162 partly contact each other, said lower electrode 164-181 is connected to said second metal layer 162 along at only an entire bottom of said lower electrode 164-181 and at no other portion, to said second metal layer 162 and said lower electrode 164-181 has a thickness (60 nm, again note column 8 line 66) of 30 nm or greater at the bottom portion 164 of said lower electrode 164-181. Note figures 2,3,14-19, column 3 lines 19-23, column 8 lines 14-67, and column 9 lines 1-45 of Torii et al.

C. With regard to claims 49,50, and 52 the third example of Torii et al. discloses a semiconductor MIM capacitor comprising a cup shape lower electrode 164-181 electrically connected to a metal layer 101 at a bottom portion 164 of said lower electrode 164-181, said lower electrode 164-181 formed on a bottom of a hole and a side wall surface of the hole in an insulating interlayer film 161-171 (Torii et al. make

their insulating interlayer film in two steps, covering the lower film 161 of figure 16 with an upper film 171 in figure 17); a capacitive insulating film 131 formed on said lower electrode 164-181; and an upper electrode 132 formed on said capacitive insulating film 131, wherein said bottom portion 164 of said lower electrode 164-181 has a thickness (60 nm, note column 8 line 66) greater than a side wall portion 181 (only 50 nm thick, note column 9 line 50) of said lower electrode 164-181, and wherein the entire portion of said bottom portion 164 of said lower electrode 164-181 is connected to said metal layer 101. Note figures 2,3,14-19, column 3 lines 19-23, column 8 lines 14-67, and column 9 lines 1-45 of Torii et al.

Allowable Subject Matter

3. Claims 3,9, and 53-62 are allowed over the references of record for the reasons set forth, with respect to independent claims 3 and 9, in the paper mailed 12/28/05. It is further noted that every embodiment of Torii et al. has lower electrodes having side wall portions of 30 nm thickness (or more), a thickness prohibited by claims 3 and 9.

4. Claim 51 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

5. Applicant's arguments with respect to claims 2,8,15,16,18-20,49,50 and 52 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you

have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thomas L. Dickey
Patent Examiner
Art Unit 2826
05/06